DEC STD 184-0 PROGRAMMABLE INTEGRATED CIRCUIT DOCUMENTATION: PROCESS AND REQUIREMENTS

DOCUMENT IDENTIFIER: A-DS-EL00184-00-0 Rev D, 20-Nov-1989

ABSTRACT: This document specifies the requirements and process for the generation and release of specific design options for programmable integrated circuits. In addition, it includes all programmable, integrated circuit devices within Digital with the class part number of 23.

APPLICABILITY: This standard encompasses all memory and logic technologies that receive 23-class Digital part numbers. New pattern releases must meet the requirements specified in this document. All design and component engineers who work with programmable devices are required to comply with this standard.

STATUS: APPROVED 20-Nov-1989; use VTX SMC for current status.

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1 INTRODUCTION

1.1 PURPOSE

DEC STD 184-0 specifies the requirements and process for the generation and release of specific design options for programmable integrated circuits. This document addresses the following areas.

— The process for pattern development

— The requirements for testability for programmable logic devices

— The process for pattern release that allows devices to be programmed, tested, and shipped to manufacturing sites

— The responsibilities of the design and component engineer and Semiconductor Business Operation (SBO) Document Control personnel at each step of the process

— The documentation to be archived for each specific design option

In addition, this standard includes all programmable, integrated circuit devices within Digital with the class part number of 23. The following memory and logic device families are included.

ROM	-	Read Only Memory
PROM	-	Programmable Read Only Memory
EPROM	-	Erasable Programmable Read Only Memory
PAL	-	Programmable Array Logic
FPLA	-	Field Programmable Logic Array
FPLS	-	Field Programmable Logic Sequencer
LCA	-	Logic Cell Array

1.2 SCOPE

This standard encompasses all future programmable memory and logic technologies that receive 23-class Digital part numbers. New pattern releases must meet the specified requirements. All design and component engineers working with programmable devices are required to comply with this standard.

Design documentation created prior to the approval of this standard need not be revised to meet the new requirements.

Flow charts and process descriptions are provided to help the design engineer understand how engineering support groups function in the programmable device development and release process. This standard describes this process in sequence, lists the responsible groups, when to contact them, the inputs they require, and the services they provide.

2 DEVELOPMENT

2.1 DESIGN TOOLS

Selecting the appropriate design tool depends upon the particular device to be configured by the designer.

To obtain a design tool, install the "PLCAD ENVIRONMENT" within the VMS environment by extracting the command file from the VAXnotes conference: "PLDVAX::23class_semiconductor". After extracting the file, run it at the VMS level.

"PLCAD" is delivered to the account overnight. The toolbox contains utilities necessary to obtain PLD design tools. The utilities in the "PLCAD" are:

Table 1: Table of PLCAD Utilities

Utility	Description
HELP	An online method of getting help on PLCAD functions and design tools.
RECALL	A recall function similar to VMS recall that recovers previously entered command lines.
REQUEST	A function used by the PLCAD manager to copy a backup saveset containing a specific design tool.
INSTALL	A function used by the PLCAD manager to install a requested design tool saveset.
TESTABILITY	A method for checking the Testability of a PLD.
NODE	The ability to add, delete or list nodes in the node access list.
RELEASE	This function is used only after the 23 class device is designed and verified by the designer. This function sends the proper files by NMAIL to ANT::23RELEASE. Only CUPL, FPLS, and ROMgen version 5 generated files will use this function.

If PLCAD is installed, the user must then REQUEST a saveset and INSTALL the desired tools within PLCAD. (Online Help is available.)

Each of the functions are "tools" used to design code-files to configure a device. These design tools generate appropriate code-files for simulation, device programming, and subsequent release.

Table 2: Table of Optional PLCAD Tools That Must Be Requested

Tool	Description
CUPL	Compiler used for PLDs design entry
CSIM	Simulator for designs created using CUPL
ALDG	Automatic Logic Diagram Generator, generates logic diagrams for most PLDs from a JEDEC file
FPLS	Compiler used for FPLS PLDs design entry
FPLSIM	Simulator for FPLS type devices (L1, L3, and 82S168)
ROMGEN	Used for designing ROMs
SA	State Assignment Program for state machines. FPLS compatible

2.2 TESTABILITY

Using the testability feature ensures that the designer uses preferred design techniques. Note that the release process will flow smoothly by verifying a high testability value.

Execute the command PLCAD TESTABILITY {NNNQQ}, where:

- NNN is any 3-digit number or letter-number code followed by a 2-digit number.
- QQ is a letter-number code corresponding to the base Digital part number of the PLD.
- NNNQQ.JDC is a file in the user area.

A mail message is delivered indicating whether the device is testable, according to the fault-grading software used to generate test vectors.

If the design is not testable, the mail message provides suggestions for necessary corrections. The designer may either change the design and perform the function again, or generate test initialization sequences before the design is RELEASED to production.

NOTE

Failure to provide a testable design, or to test initialization sequences with the design, will cause substantial delay and extra cost.

2.3 PROTOTYPE VERIFICATION

Prototype verification, by the designer, is recommended. It should consist of either one or both of the following.

- Simulation of the device in the modeled assembly
- Physical insertion of the configured device into a prototype assembly

2.4 OBTAINING PARTS

To configure sample units to a particular design, contact a customer service representative at the Semiconductor Business Operation (SBO). The required number of parts are programmed according to the device code supplied. An outgoing electrical test is not performed on these devices. Special Project parts are supplied "as is."

2.5 POLICY ON OUTSIDE DISTRIBUTORS

SBO policy does not support the use of outside distributors.

2.6 OBTAINING A PART NUMBER REQUEST FORM (PNRF)

Establish the approximate number and type of programmable devices to be used. Submit a PNRF for each device. The PNRFs should be submitted not more than six months in advance of the expected release of the design code file. A part number is assigned in the form 23-NNNQQ-00, with an associated base part number of 23-000QQ-VV. (NNN is a unique 3-digit number, QQ is a letter-number code indicating the base architecture of the device, and VV is the base device variation associated with a speed or package.)

3 RELEASE REQUIREMENTS

There are three components of the Release Requirements.

- Device Preparation
- Release Function
- Purchase Specification

3.1 DEVICE PREPARATION

Program four copies of the device to be released and mark the devices with the assigned Digital part number. (This number can be found on the copy of the PNRF.) Mark the device with an adhesive label or other means so that the vendor marking can be seen.

Send the devices to Specification Control in LMO2-1/O24. The mailing method shall include a Shipping Authorization. These device copies will become the standard for use in verifying the device test program after the Release is completed. Refer to *DEC STD 067-0 Handling of Electrostatic-Sensitive Devices - Procedures and Protective Materials*.

3.2 RELEASE FUNCTION

For the design system, execute the PLCAD RELEASE command using the appropriate part number syntax:

FORMAT COMMAND	PLCAD RELEASE
PARAMETERS	**DEC_part_number**
	Digital part number 23-000BB-00, 23-000BB, or 000BB
QUALIFIERS	**/Flags**
	This parameter is used if the device being released was generated with the CUPL compiler. This parameter should contain the same flags used in the last PLCAD CUPL compile run.
	/CUPL
	This qualifier specifies that the device being released was generated using the CUPL compiler. This qualifier cannot be used with /CUPL or /ROMGEN.
	/FPLS
	This qualifier specifies that the device being released was generated using the FPLS compiler. This qualifier cannot be used with /CUPL or /ROMGEN.
	/ROMGEN
	This qualifier specifies that the device being released was generated using the ROMGEN compiler. This qualifier can not be used with /CUPL or /FPLS.
DESCRIPTION	This function sends the proper files by electronic mail to ANT::23RELEASE. Use this function when the device has been designed and verified.

3.2.1 For FPLSs

The standard release file for FPLSs is the ".PPT" output file created by the FPLS program. The release file name for FPLS patterns shall be "XXXXX.PPT" where XXXXX is the 5-character basic part of the pattern number. The input file for FPLS is called the ".PLS" file.

The PLCAD RELEASE "DEC_part_number" shall contain the dash variation of the base device. For example, if 23-000L1-03 is the base device and the assigned pattern number is 23-123L1-00, use 23-123L1-03.

3.2.2 For ROM/PROMs

The standard release files for ROM/PROMs are the industry standard Intel HEX (MDS8 or MCS86) or Motorola HEX (EXORCISER or EXORMAX) formats with pattern control inserted at the top of the file before the start of any data. Use ROMGEN to create this file to ensure that the pattern control information is written correctly.

The release file name for these patterns is XXXXX.RELEASE where XXXXX is the 5-character part of the pattern number.

3.2.3 For PLDs Processed by CUPL

When using PLCAD RELEASE, the name field in the .PLD file is the 5-digit Digital part number (Name 001J5). The .PLD file must be run through CUPL before attempting to RELEASE.

The PLCAD RELEASE "DEC_part_number" shall contain the dash variation of the base device. For example, if 23-000K8-04 is the base device and the assigned pattern number is 23-123K8-00, use 23-123K8-04.

3.2.4 For Flags Processed by CUPL

The flag parameter is used if the device being released is generated with the CUPL compiler. It shall contain the same flags used in the PLCAD CUPL compile run, which are used to generate the final version of the device.

3.3 PURCHASE SPECIFICATION

Sign the specification in the appropriate place and return to the 23 Class Coordinator of Specification Control. The purchase specification may be sent by interoffice mail, or may be included with the devices.

NOTE

The three steps in the RELEASE REQUIREMENTS section must be completed in-order to deliver the design to manufacturing.

The following steps allow delivery of the design-to-manufacturing process.

1. Send prepared devices. Refer to 3.1.
2. VAXmail device design. Refer to 3.2.
3. Send signed specification. Refer to 3.3.

3.4 PATTERN VERIFICATION

Pattern Verification is a Quality Control step in the release process. Upon receipt of the prepared devices and the VAXmailed device design, Quality Control loads the code into a device programmer and performs a verify function with each device.

In the event that a failure occurs at this point, the designer is notified that the design release has failed and the designer must re-initiate the release process.

3.5 MASK ROM, HAL RELEASE PROCESS

This release process is transparent to the designer, and focused at the manufacturing buyer. When it is determined that a device has sufficient volume, a Pattern Verification Traveller is initiated by the buyer. Refer to Figure 1.

Enter the Digital part number and Supplier Name on the Pattern Verification Traveller, and start the signature process. Each of the following steps must be initialized and dated on the Traveller. Refer to Figure 1.

1. Request master device and develop pattern specification.
2. Supply device and specification.
3. Send device and specification to supplier.
4. Supplier indicates receipt and programs two devices.
5. Receive devices from supplier.
6. Request supplier device verification.
7. Initiate master verification.
8. Distribute copies.

Upon completion, the buyer orders preprogrammed devices from the supplier.

Figure 1: Pattern Verification Traveller

DIGITAL PART NUMBER_____

VENDOR_____

SIGNATURE AUTHORIZATIONS

1. SBO Purchasing–Requested Masters and Pattern Specification from SBO Document Control.

   Purchasing:_____Date:_____

   LM02 Document Control:_____ Date:_____

2. SBO Document Control–Supplied Masters and Pattern Specification to SBO Purchasing.

   Document Control:_____ Date:_____

   Purchasing:_____ Date:_____

3. SBO Purchasing–Sent Masters and Pattern Specification to Vendor.

   Purchasing:_____ Date:_____

4. Vendor–Received Masters and Blasts Two Additional Vendor Masters.

   Vendor_____

   Name and Title:_____Date:_____

5. SBO Purchasing–Received Vendor–Masters from Vendor.

   Purchasing:_____Date:_____

6. SBO Purchasing–Requested Verification From SBO Document Control.

   Purchasing:_____Date:_____

   Document Control:_____ Date:_____

7. SBO Document Control–Verified Vendor Masters and returns this Pattern Verification Form to SBO Purchasing.

   Document Control:_____ Date:_____

   Purchasing:_____ Date:_____

8. SBO Purchasing will distribute copies of this form to SBO Purchasing. SBO Document Control and the above Vendor.

3.6 EXPIRATION

Designers are responsible for inactivating 23-class part patterns on canceled projects.

The PNRFs should be submitted not more than 10 months in advance of the time the designer expects to release the PNRFs. A designer is provided with a part number in the form 23-NNNQQ-00.

If the PNRF remains open for 10 months, an ECO is initiated to inactivate the part number. A warning shall be issued in advance of the expiration deadline. The expiration deadline allows Specification Control to purge documents for canceled projects.

It is the component engineer's responsibility to sign off the inactivation ECO. This ensures that parts associated with active projects are not inactivated.

4 ARCHIVE REQUIREMENTS

Verified pattern files are stored in the Engineering Support Library. Files may be obtained upon request at DTN 225-4273 or sent in writing via VAXmail to STUDIO::HULL.

5 PATTERN CHANGE REQUIREMENTS

Once a 23-class purchase specification number has been approved and released, the programmable device pattern defined by that 23-class number must not be changed.

To obtain a new or replacement programmable device pattern, a new 23-class number must be requested and assigned in accordance with *DEC STD 012-2 Unifed Numbering Code For Part Identifier Class Codes*. The appropriate change orders must be initiated to introduce the new part and to change the status of the old parts in the affected documentation and accounting systems.

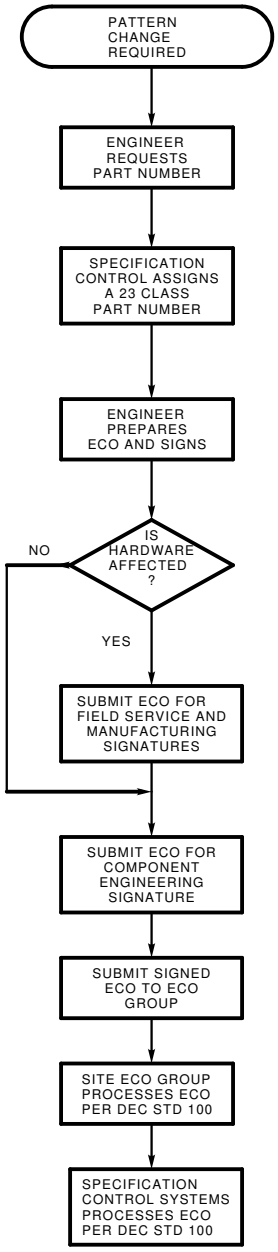
When a pattern change does not affect specific module documentation, a purchase specification ECO per *DEC STD 100-0 Policy and Requirements for the Product Change Process* is the only change document required. For example, the M9312 module is shipped with empty sockets. Therefore, pattern changes do not affect the M9312 package.

When a pattern change affects specific module applications or the status of existing parts, the module hardware and associated documentation must be changed.

5.1 ECO PROCESS

The flow chart in Figure 2 shows the process involved when using the single hardware ECO to change the pattern requirements on a module and to accommodate the Purchase Specification ECO requirements. Figure 2 describes the process and specifies any requirements the design engineer and support groups must fulfill to enable this process.

Figure 2: Pattern Change Process Flow Diagram


PATTERN CHANGE REQUIRED
ENGINEER REQUESTS PART NUMBER
SPECIFICATION CONTROL ASSIGNS A 23 CLASS PART NUMBER
ENGINEER PREPARES ECO AND SIGNS
IS HARDWARE AFFECTED ?
NO
YES
SUBMIT ECO FOR FIELD SERVICE AND MANUFACTURING SIGNATURES
SUBMIT ECO FOR COMPONENT ENGINEERING SIGNATURE
SUBMIT SIGNED ECO TO ECO GROUP
SITE ECO GROUP PROCESSES ECO PER DEC STD 100
SPECIFICATION CONTROL SYSTEMS PROCESSES ECO PER DEC STD 100

6 ENGINEERING DOCUMENTATION REQUIREMENTS FOR PATTERNS

Programmable device pattern information, such as ROM listings, is not normally listed as a drawing in engineering documentation for a module unless specifically required by the design engineer. When this requirement is specified, the pattern information to be referenced is identified by entering the Specification Control Systems' Pattern Specification document number (with an A-PS-23XXXXX-0-0 document identifier) on the Drawing Directory (DD) for the module.

APPENDIX A

REFERENCED DOCUMENTS

A.1 EL-Class Digital Documents

EL-Class Number	Document Title
EL-00012-02	*DEC STD 012-02 Unifed Numbering Code For Part Identifer Class Codes*
EL-00067-00	*DEC STD 067-0 Handling of Electrostatic-Sensitive Devices - Procedures and Protective Materials*
EL-00100-00	*DEC STD 100-0 Policy and Requirements for the Product Change Process*
EL-00100-01	*DEC STD 100-1 Engineering Change Orders - Hardware*

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